SYNCHRONOUS RECTIFYING CONTROL CIRCUIT OF FLYBACK SWITCHING POWER SUPPLY

Field of the invention

The present invention relates to a synchronous rectifying control circuit of a flyback switching power supply and, more particularly, to a control circuit used on a secondary side circuit of a flyback switching power supply and capable of synchronously controlling a plurality of sets of rectifying outputs and synchronously adjusting the waveforms of rectifying outputs.

Background of the invention

In existent DC power supply devices like AC to DC switching power supplies, in order to shrink the volume, a high-frequency pulse width modulation (PWM) controller is exploited to control the DC output voltage. As shown in Fig. 1, the front-stage circuit and the rear-stage circuit of a transformer T1 are divided into a primary side 101 and a secondary side 102. A phototransistor 111 and a photodiode 112 between the primary side 101 and the secondary side 102 are used to separate electric signals of the primary side 101

and the secondary side 102. Optical signals can be used to feed back the voltage or current output variation signal of the secondary side 102 to the primary side 101 for synchronous adjustment of the voltage and current variation of the primary side 101 and the secondary side 102, or can be used as feedback signals for over-current and short-circuit protection.

In the prior art, a flyback power supply is primarily a circuit for converting an AC voltage into a DC voltage. It is based on the following principle. When a field-effect transistor (FET) Q1 on the primary side 101 conducts, energy cannot be transferred through a rectifying diode D1 due to polarity inversion of the primary side and the secondary side, and is stored on the transformer T1. After the conduction period of the FET Q1 is over, the polarity of the transformer T1 inverses, and the rectifying diode D1 on the secondary side conducts to release energy stored on the transformer T1. However, when the rectifying diode D1 conducts, there is a voltage drop of about 0.4-1.5V according to the magnitude of the output load. This voltage drop multiplied by the load current is the dissipation power loss of the rectifying diode D1. If the

load current is large, the output power source efficiency of the DC power supply device is much reduced.

For an existent flyback switching power supply, there generally is more than one set of output power sources. If all the output power sources are to have synchronous output voltages and waveforms, a very complicated circuit is required. Therefore, in order to save costs, most of existent flyback switching power supplies have no synchronous output function, and the output voltages and waveforms thereof need to be adjusted separately.

SUMMARY OF THE INVENTION

The primary object of the present invention is to provide a synchronous rectifying control circuit of a flyback switching power supply, which is connected at a secondary side of a transformer and has a plurality of sets of power source ends and a set of induction ends. The power source ends comprise a first power source output end and a secondary power source output end. The set of induction ends comprises a first induction end and a second induction end. The secondary power source output end of the power source

ends is connected to a rectifying circuit for rectifying the voltage waveform between the first power source output end of the power source ends and a reference potential end. The first induction end of the set of induction ends is connected to a rectifying diode, which is used to rectify the first induction end and the reference potential end to form a detection end having a waveform with the same phase as the power source ends. A synchronous control circuit is connected to the first power source output and the detection end, and comprises a synchronous input end, a control end and a waveform adjustment end. The synchronous input end is used for input of a synchronous signal. The control end is connected to the rectifying circuit and used to synchronously control the rectifying circuit to generate a uniform rectifying response period, hence accomplishing synchronous adjustment of several sets of output voltage waveforms.

Another object of the present invention is to provide a synchronous rectifying control circuit of a flyback switching power supply, wherein a comparator is provided. The comparator has a positive input end, a negative

input end and an output end. The positive input end connects a first resistor to the detection end and connects a second resistor to the reference potential end. The negative input end connects a third resistor to the first power source output end and connects a fourth resistor to the reference potential end. The output end connects a fifth resistor for feedback to the positive input end to convert the waveform of the detection end into a waveform having an apparent slope, hence accomplishing synchronous adjustment of the control circuit to increase or decrease the response period of the rectifying circuit.

Yet another object of the present invention is to provide a synchronous rectifying control circuit of a flyback switching power supply, which is connected at a secondary side of a transformer and has a plurality of sets of power source ends and a set of induction ends. The power source ends comprise a first power source output end and a secondary power source output end. The set of induction ends comprises a first induction end and a second induction end. The drain (D) of an FET is connected to the second power source output end and the source (S) of the FET is connected to a reference

potential end so that the voltage waveform between the first power source output end and the reference potential end can be rectified through conducting or shutting off the FET. The first induction end is connected to a rectifying diode to rectify the first induction end and the reference potential end to form a detection end having a waveform with the same phase as the first power source output end. A comparator is used to convert the waveform at the detection end into a waveform having an apparent slope. A drive control circuit has a control input end and a control output end. The control input end is connected to the output end of the comparator and the control output end is connected to a gate (G) of the FET to drive and control the FET for increasing or decreasing the rectifying response period.

BRIEF DESCRIPTION OF THE DRAWINGS

The various objects and advantages of the present invention will be more readily understood from the following detailed description when read in conjunction with the appended drawing, in which:

Fig. 1 is a circuit diagram of a conventional flyback switching power supply;

Fig. 2 is a circuit diagram according to a first embodiment of the present invention;

Fig. 3 is a circuit diagram according to a second embodiment of the present invention;

Fig. 4 is a waveform diagram of a control circuit of the present invention;

Fig. 5 is an internal circuit diagram of an IC according to the first embodiment of the present invention; and

Fig. 6 is an internal circuit diagram of an IC according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As shown in Figs. 2, 3 and 4, the present invention provides a control circuit, which mainly applies to a flyback switching power supply having a set or several sets of output power sources, and is used to synchronously control the voltage waveforms of several sets of outputs or synchronously adjust the rectifying response periods of several sets of outputs.

As shown in Fig. 2, a synchronous rectifying control circuit 10 of the present

invention is connected at a secondary side 102 of a transformer T1 in the flyback switching power supply. A plurality of power source ends is provided at the secondary side of the transformer T1. In this embodiment, the transformer T1 has two sets of output coils. A first power source output end 103 and a second power source output end 104 are provided at the power source end of each set of the output coils. An induction end having a set of output coils and provided at the secondary side of the transformer T1 has a first induction end 105 and a second induction end 106. The second induction end 106 is a reference potential end, and can be a ground end.

The synchronous rectifying control circuit of the present invention mainly comprises a plurality of sets of rectifying circuits 10 and a synchronous control circuit 11. The plurality of sets of rectifying circuits 10 are respectively connected to the second power source output ends 104 of the plurality of sets of power source ends, and are used to rectify and output the voltage waveforms between the first power source output ends 103 and the reference potential end 106. The rectifying circuit 10 is composed of an FET Q1 and a diode D1. The

diode D1 is shunted between a source (S) and a drain (D) of the FET Q1. The source (S) of the FET Q1 is connected to the positive pole of the diode D1, and is also connected to the reference potential end 106. The drain (D) of the FET Q1 is connected to the negative pole of the diode D1, and is also connected to the second power source output end 104 of the power source end. The first induction end 105 of the induction ends connects a rectifying diode D2 to rectify the output power source between the first induction end 105 and the reference potential end 106 to form a detection end 107 having a waveform with the same phase as the power source end.

The synchronous control circuit 11 is connected to the first power source output end 103 and the detection end 107, and comprises a first synchronous input end 108, a control end 109 and a waveform adjustment end 110. The synchronous input end 108 is used for input of a synchronous signal. The synchronous signal is generated by a PWM controller at the primary side 101 of the transformer T1. The control end 109 is connected to a gate (G) of the FET Q1 in the plurality sets of rectifying circuits 10, and is used to

synchronously control the rectifying circuits 10 to generate a uniform rectifying response period.

The waveform adjustment end 110 can be externally connected to a resistor for adjusting its DC voltage to change the voltage waveform on the control end 109 and control the on or off response period of the FET Q1, thereby reducing or increasing the synchronous rectifying response period. If the waveform adjustment end 110 connects a resistor to the first power source output end 103, the synchronous rectifying response period of the rectifying circuit 10 can be reduced. If the waveform adjustment end 110 connects a resistor to the reference potential end 106, the synchronous rectifying response period of the rectifying circuit 10 can be increased.

The synchronous control circuit 11 is composed of a comparison circuit 12 and a synchronous drive circuit 13. The comparison circuit 12 has a comparator U1, which has a positive input end U+, a negative input end U-, and an output end Uout. The positive input end U+ connects a first resistor R3 to the detection end 107, and connects a second resistor R4 to the reference potential

end 106. The negative input end U- connects a third resistor R1 to the first power source output end 103, and connects a fourth resistor R2 to the reference potential end 106. The output end Uout connects a fifth resistor R5 for feedback to the positive input end U+ to convert the waveform of the detection end 107 into a more ideal waveform having an apparent slope.

The synchronous drive circuit 13 is composed of transistors Q2, Q3, Q4 and Q5. The base of the transistor Q2 is connected to the output end Uout of the comparator U1, the emitter thereof is connected to the base of the transistor Q3, and the collector thereof is connected to the collector of the transistor Q3 and then to the first power source output end 103. The emitter of the transistor Q3 is connected to the emitter of the transistor Q4 and then to the collector of the transistor Q5 to form the control end. The base of the transistor Q4 is connected to the output end of the comparator U1 to form the synchronous input end 108. The collector of the transistor Q4 is connected to the base of the transistor Q5. The emitter of the transistor Q5 is connected to the reference potential end. The synchronous drive circuit 13 can thus accept potential control of the output end

Uout of the comparator U1 and the synchronous control of the synchronous input end 108 to let the FET Q1 be on or off, hence generating a synchronous rectifying response period. Fig. 4 shows the response period waveforms of the detection end 107, the waveform adjustment end 110 and the FET Q1 in the control circuit. The potential of the waveform adjustment end 110 can be used to adjust the conduction period of the transistor Q1.

In the first embodiment of the present invention, the comparison circuit 12 and the synchronous drive circuit 13 in the control circuit 11 can be packaged into an IC with eight pins. The internal circuit of the IC is shown in Fig. 5. The pins at least comprises a power source pin Vcc (103), a ground pin GND (106), a detection end pin DETECT (107), a waveform adjustment end pin ADJUST (110), a synchronous input end pin SYNC (108) and a control end pin OUTPUT (109).

As a second embodiment shown in Fig. 3, the control circuit of the present invention can also apply to a circuit having a single output power source. It differs from the first embodiment only in that the synchronous signal input end

is omitted. The control circuit of the second embodiment can be packaged into an IC with five pins. In order to lower the cost of circuit, the FET is also packaged into the IC. The internal circuit is shown in Fig. 6. The pins at least comprises a power source pin Vcc (103), a ground pin GND (106), a detection end pin DETECT (107), a waveform adjustment end pin ADJUST (110) and a rectifying output end pin DRAIN (104).

Although the present invention has been described with reference to the preferred embodiment thereof, it will be understood that the invention is not limited to the details thereof. Various substitutions and modifications have been suggested in the foregoing description, and other will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.